**FAULT TOLERANT KMD GATES**

Parity checking is one of the broadly used method for error detection in digital systems. It is normally used for detecting errors in the storage or transmission of data, essentially because most arithmetic and other processing function do not safeguard the parity of the information.

A reversible gate is said to be parity preserving when the XOR operation on input vectors Iv= {I1, I2, ……., In} is same as the XOR operation on output vectors Ov= {O1, O2, …., On}.

I1 ⊕ I2 ⊕ ..... ⊕ In-1 ⊕ In = O1 ⊕ O2 ⊕ ….. ⊕ On-1 ⊕ On ……….. (1)

A circuit is known as parity preserving only when it is constructed using the parity preserving gates [14]. Fault tolerance is the property of the system that permit a system to work continuously even in the failure of some of its components. The fault coverage and fault tolerance of KMD Gates are discussed in this chapter.

**STUCK-AT FAULT**

In stuck-at fault model, fault occurred in a circuit when any wire fixed on a value ‘0’ or ‘1’, called as stuck-at 0 or stuck-at 1 fault respectively. Total number of stuck-at faults can be obtained by [8],

Where, gi represents the size of Nth gate of the circuit, n represents the total number of wires and m represents the number of gates in the circuit.

**TEST VECTOR GENERATION AND FAULT COVERAGE OF KMD GATES**

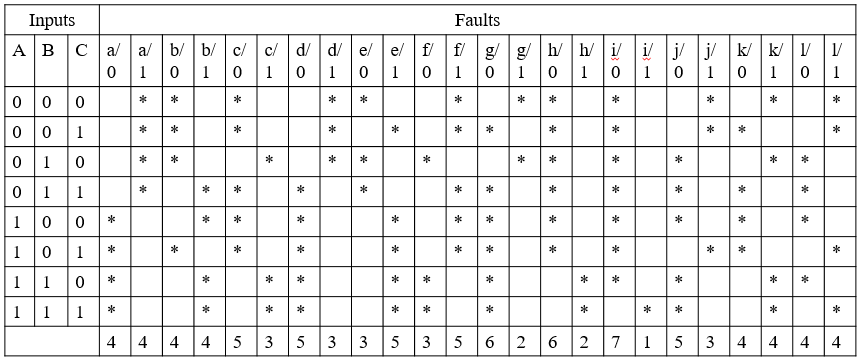
**1. KMD Gate1**

The test vectors of the circuit or gate is identified using fault table analysis. The fault table analysis for the test vector generation of KMD Gate1 is shown in Table 1. Using this table, an input capable of covering the maximum number of fault is chosen as the test vector. A set of test vectors which covers all the fault is known as test set. These test set is used to check the functionality of the KMD Gate1whether it is good or faulty.

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| **Figure 1(a): Block diagram of KMD Gate 1** | **Figure 1(b): Quantum Equivalent of KMD Gate 1** |
|  | |
| **Figure 1(c): Logic Diagram of KMD Gate 1** | |

The block diagram and the Quantum Equivalent circuit of KMD Gate 1 is shown in Figure 1 (a) and (b). In the Figure 1(c) denotes the possible locations of the fault.

**Table 1: Fault Table of KMD Gate1**



**Minimum test vectors**

The minimum test vectors are the test a vector covering maximum number of faults occurs in the reversible circuit and its detectable faults are listed below

000 – a/1 b/0 c/0 d/1 e/0 f/1 g/1 h/0 i/0 j/1 k/1 l/1

011 – a/1 b/1 c/0 d/0 e/0 f/1 g/0 h/0 i/0 j/0 k/0 l/0

111 – a/0 b/1 c/1 d/0 e/1 f/0 g/0 h/1 i/1 j/0 k/1 l/1

Here this three minimum test vector covers all the fault in the KMD Gate1 thus, to detect the fault in the gate.

**Test Vector** = {000, 011, 111}

**Fault Coverage**

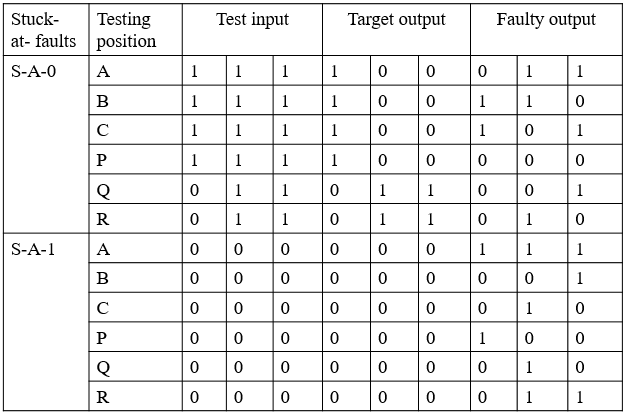
Fault coverage shows the test vectors after removing redundancy from the above

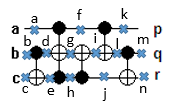
000 – A/1 B/0 C/0 P/1 Q/1 R/1 = 6/12

011 – Q/0 R/0 = 2/12

111 – A/0 B/1 C/1 P/0 = 4/12

**Table 2 Fault Coverage table of KMD Gate1**



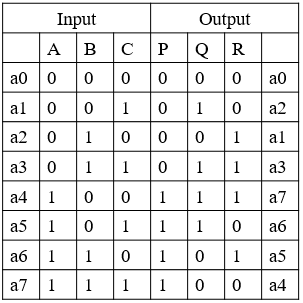
**Fault Tolerant**

where indicates the possible position of faults

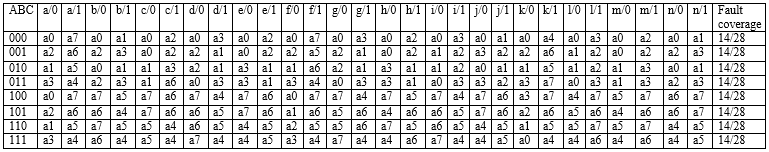
**Figure 2: Quantum Equivalent of KMD Gate 1 with possible stuck-at fault points**

The truth table of KMD Gate1 is shown in Table 3 and its fault tolerance capability is analyzed in Table 4. Here a0 to a7 represent the position of the i/o vector.

**Table 3: Truth Table of KMD Gate1**



**Table 4: Fault tolerant table of KMD Gate1**



From the table the average Fault tolerant of KMD Gate1 is 50 %

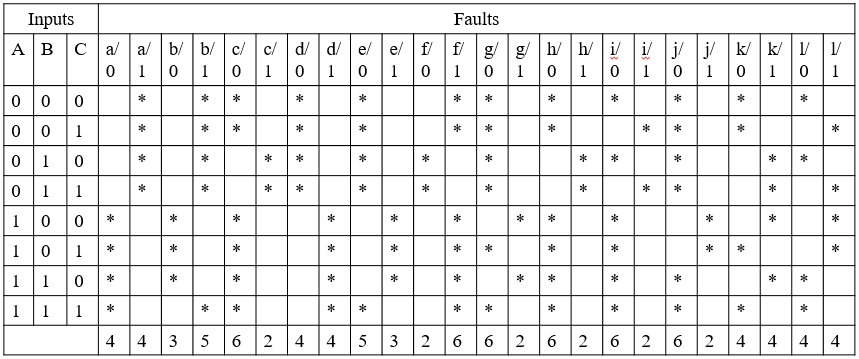
**2. KMD Gate2**

The test vectors of the circuit or gate is identified by using fault table analysis. The fault table analysis for the test vector generation of KMD Gate2 is shown in Table 5. Using this table, an input capable of covering the maximum number of fault is chosen as the test vector. A set of test vectors which detects all the faults is known as test set. These test set is used to check the functionality of the KMD Gate1whether it is good or faulty.

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| **Figure 3(a): Block diagram of KMD Gate2** | **Figure 3(b): Quantum Equivalent of KMD Gate2** |
|  | |
| **Figure 3(c): Logic Diagram of KMD Gate2** | |

The block diagram and the Quantum Equivalent circuit of KMD Gate 2 is shown in Figure 3 (a) and (b). In the Figure 3(c) denotes the possible locations of the fault.

**Table 5: Fault Table of KMD Gate2**



**Minimum Test Vectors**

The minimum test vectors are the test vectors covering maximum faults occur in the reversible circuit and its detectable faults are listed below

000 – a/1 b/1 c/0 d/0 e/0 f/1 g/0 h/0 i/0 j/0 k/0 l/0

100 – a/0 b/0 c/0 d/1 e/1 f/1 g/1 h/0 i/0 j/1 k/1 l/1

011 – a/1 b/1 c/1 d/0 e/0 f/0 g/0 h/1 i/1 j/0 k/1 l/1

Here this three minimum test vector covers the entire fault in the KMD Gate 2 thus, to detect the fault in the gate.

**Test Vector=** {000, 100, 011}

**Fault Coverage**

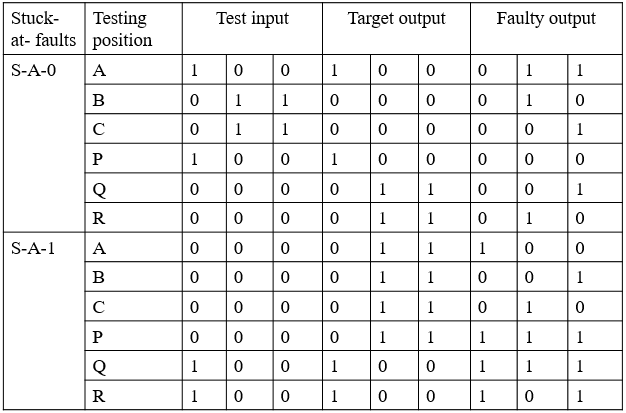
Fault coverage shows the test vectors after removing redundancy from the above

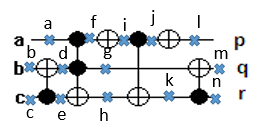
000 – A/1 B/1 P/1 Q/0 R/0 = 5/12

100 – A/0 B/0 C/0 P/0 Q/1 R/1 = 6/12

011 – C/1 = 1/12

**Table 6 Fault Coverage table of KMD Gate2**

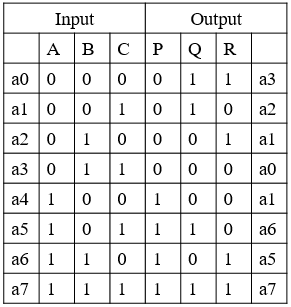


**Fault Tolerant**

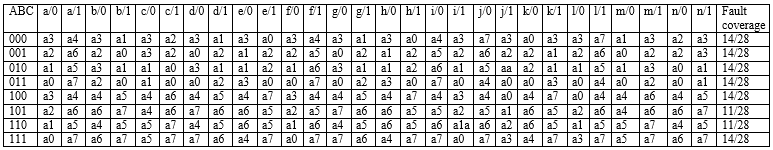
where indicates the possible position of faults

**Figure 4: Quantum Equivalent of KMD gate2 with possible stuck-at fault points**

The truth table of KMD Gate2 is shown in Table 7 and its fault tolerance capability is analyzed in Table 8. Here a0 to a7 represent the position of the i/o vector.

**Table 7: Truth Table of KMD Gate2**

**Table 8: Fault tolerant table of KMD Gate2**

From the table the average Fault Tolerance of KMD Gate2 = 47.32%

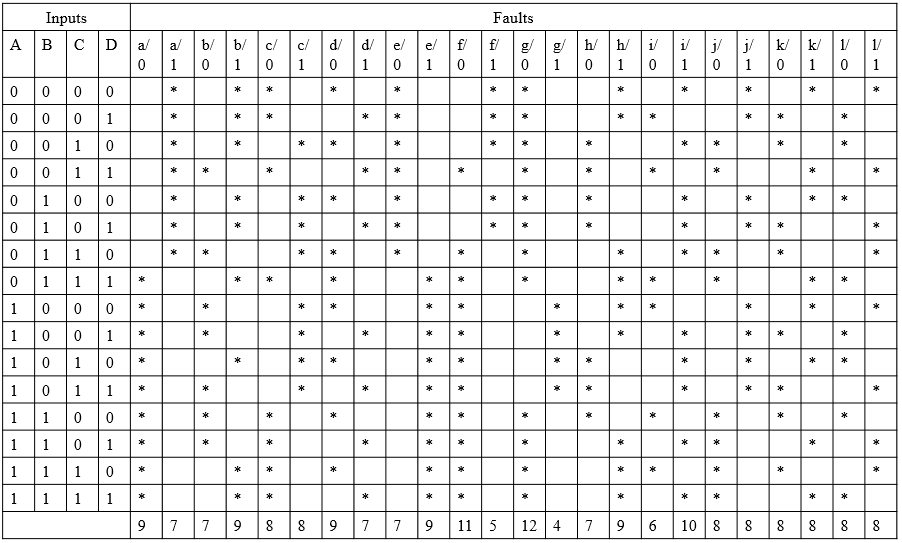
**3 KMD Gate3**

The set of test vectors which covers all the faults is known as test set. The fault table analysis for the test vector generation of KMD Gate3 is shown in Table 9. Using this table, an input capable of covering the maximum number of fault is chosen as the test vector. A set of test vectors which detects all the fault is known as test set. These test set is used to check the functionality of the KMD Gate1whether it is good or faulty.

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| **Figure 5(a): Block diagram of KMD Gate3** | **Figure 5(b): Quantum Equivalent of KMD Gate3** |
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| |  | | --- | | **Figure 5(c): Logic Diagram of KMD Gate3** | | |

The block diagram and the Quantum Equivalent circuit of KMD Gate 3 is shown in Figure 5 (a) and (b). In the Figure 5(c) denotes the possible locations of the fault.

**Table 9: Fault Table of KMD Gate3**



**Minimum Test Vectors**

The minimum test vectors are the test vectors covering maximum faults occurs in the reversible circuit and its detectable faults are listed below

0000 – a/1 b/1 c/0 d/0 e/0 f/1 g/0 h/1 i/1 j/1 k/1 l/1

0111 – a/0 b/1 c/0 d/0 e/1 f/0 g/0 h/1 i/0 j/0 k/1 l/0

1011 – a/0 b/0 c/1 d/1 e/1 f/0 g/1 h0 i/1 j/1 k/0 l/1

Here this three minimum test vector covers all the fault in the KMD Gate 3 thus, to detect the fault in the gate.

**Test Vector** = {0000, 0111, 1011}

**Fault Coverage**

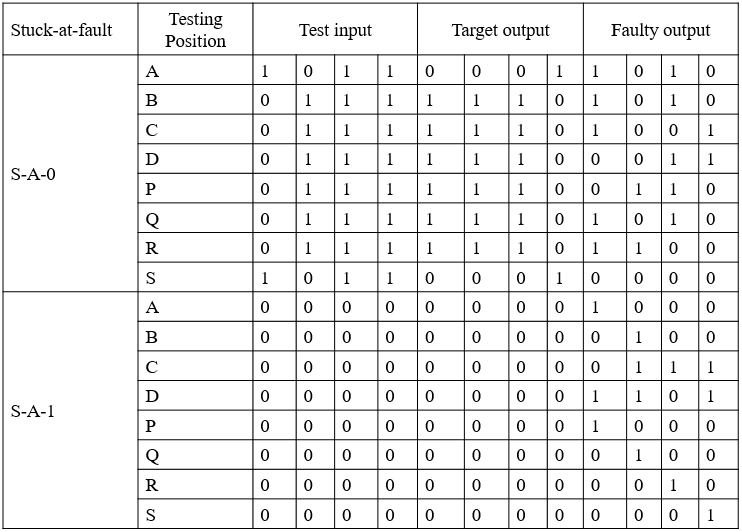
Fault coverage shows the test vectors after removing redundancy from the above

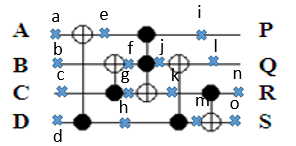
0000 – A/1 B/1 C/0 D/0 P/1 Q/1 R/1 S/1 = 8/16

0111 – A/0 P/0 Q/0 S/0 = 4/16

1011 – B/0 C/1 D/1 R/0 = 4/16

**Table 10 Fault Coverage table of KMD Gate3**



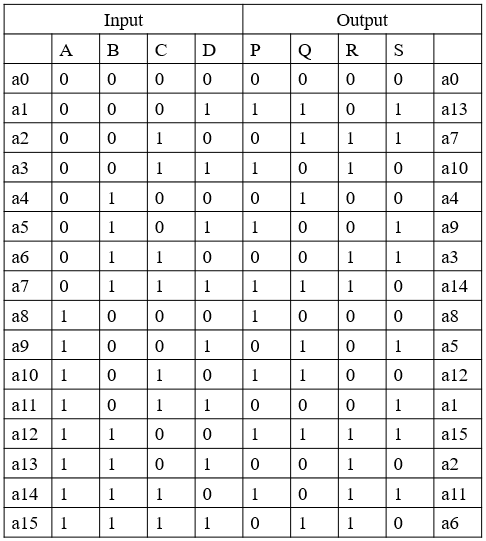
**Fault Tolerant**

where indicates the possible position of faults

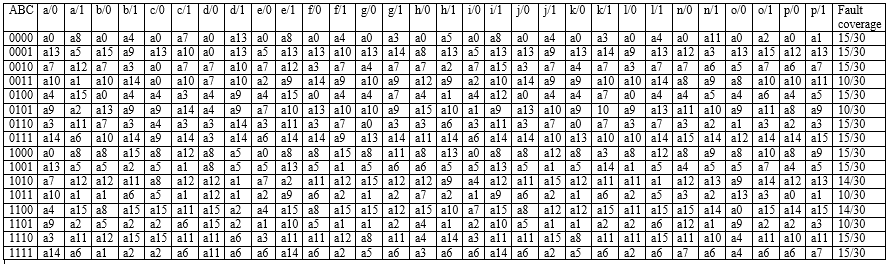
**Figure 6: Quantum Equivalent of KMD Gate3 with possible stuck-at fault points**

The truth table of KMD Gate3 is shown in Table 11 and its fault tolerance capability is analyzed in Table 8. Here a0 to a15 represent the position of the i/o vector.

**Table 11: Truth Table of KMD Gate3**



**Table 12: Fault tolerant table of KMD Gate3**

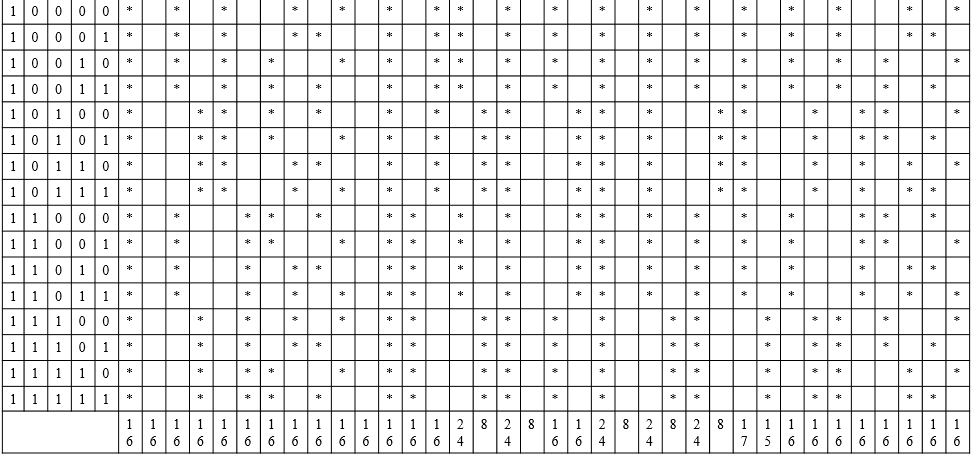


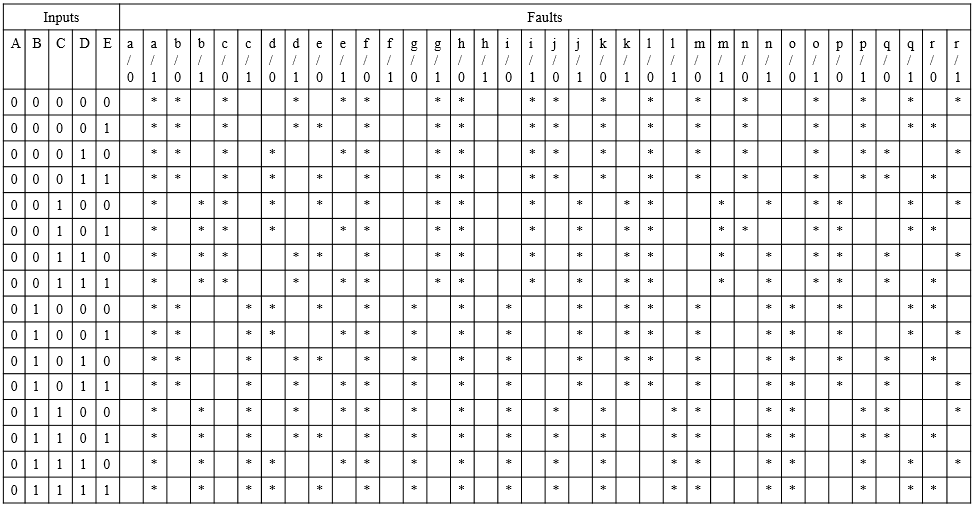
From the table the average Fault Tolerance of KMD Gate3 = 45.42%

**4. KMD Gate4**

The test vectors of the circuit or gate is identified using fault table analysis. The fault table analysis for the test vector generation of KMD Gate4 is shown in Table 13. Using this table, an input capable of covering the maximum number of fault is chosen as the test vector. A set of test vectors which detects all the faults is known as test set. These test set is used to check the functionality of the KMD Gate1whether good or faulty.

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| **Figure 7(a): Block diagram of KMD Gate4** | **Figure 7(b): Quantum Equivalent of KMD Gate4** |
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| |  | | --- | | **Figure 7(c): Logic Diagram of KMD Gate4**  The block diagram and the Quantum Equivalent circuit of KMD Gate 3 is shown in Figure 7 (a) and (b). In the Figure 7(c) denotes the possible locations of the fault. | | |

**Table 13: Fault Table of KMD Gate4**



**Minimum Test Vectors**

The minimum test vectors are the test vectors covering maximum faults occurs in the reversible circuit and its detectable faults are listed below

00000 – a/1 b/0 c/0 d/1 e/1 f/0 g/1 h/0 i/1 j/0 k/0 l/0 m/0 n/0 o/1 p/1 q/1 r/1

00100 – a/1 b/1 c/0 d/0 e/0 f/0 g/1 h/0 i/1 j/1 k/1 l/0 m/1 n/1 o/1 p/0 q/1 r/1

01100 – a/1 b/1 c/1 d/1 e/1 f/0 g/0 h/0 i/0 j/0 k/0 l/1 m/0 n/1 o/0 p/1 q/0 r/1

10111 – a/0 b/1 c/0 d/1 e/1 f/1 g/1 h/1 i/0 j/1 k/0 l/0 m/1 n/0 o/1 p/1 q/1 r/0

Here this four minimum test vector covers all the fault in the KMD Gate 3 thus, to detect the fault in the gate.

**Test Vector** = {00000, 00100, 01100, 10111}

**Fault Coverage**

Fault coverage shows the test vectors after removing redundancy from the above minimum test vectors.

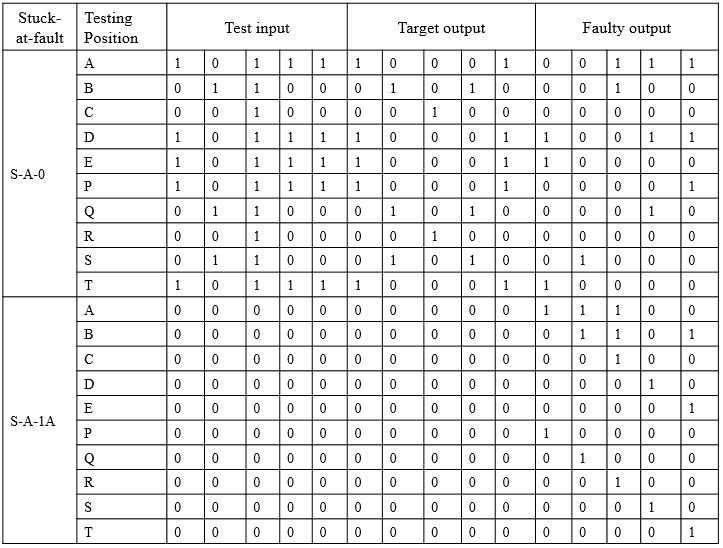
00000 – A/1 D/1 E/1 P/1 Q/1 R/1 S/1 T/1 = 8/20

00100 – B/1 C/0 D/0 E/0 R/0 = 5/20

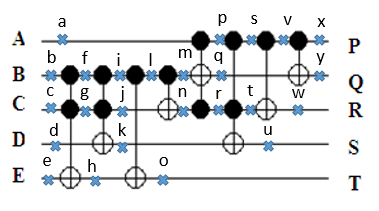
01100 – C/1 Q/0 S/0 = 3/20

10111 – A/0 P/0 T/0 = 5/20

**Table 14 Fault Coverage table of KMD Gate4**



**Fault Tolerant**

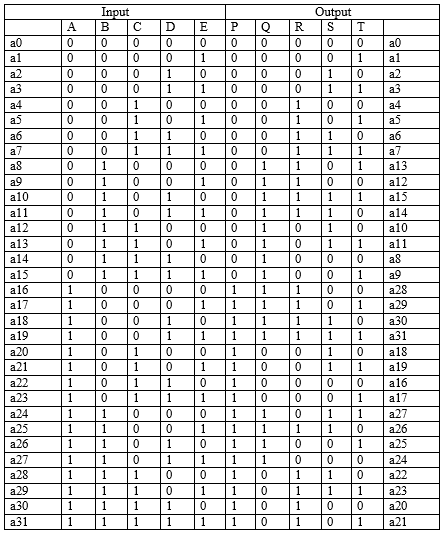
****

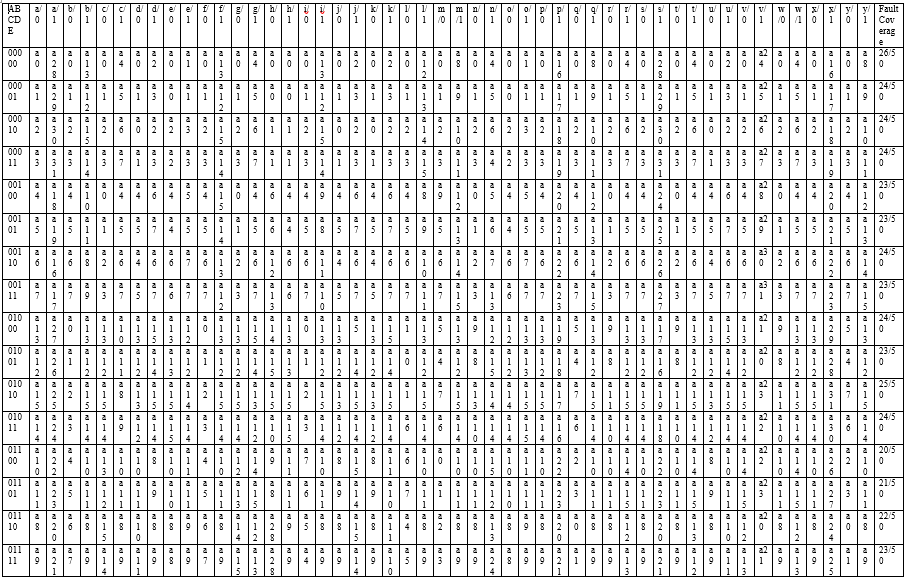
where indicates the possible position of faults

**Figure 8: Quantum Equivalent of KMD Gate3 with possible stuck-at fault points**

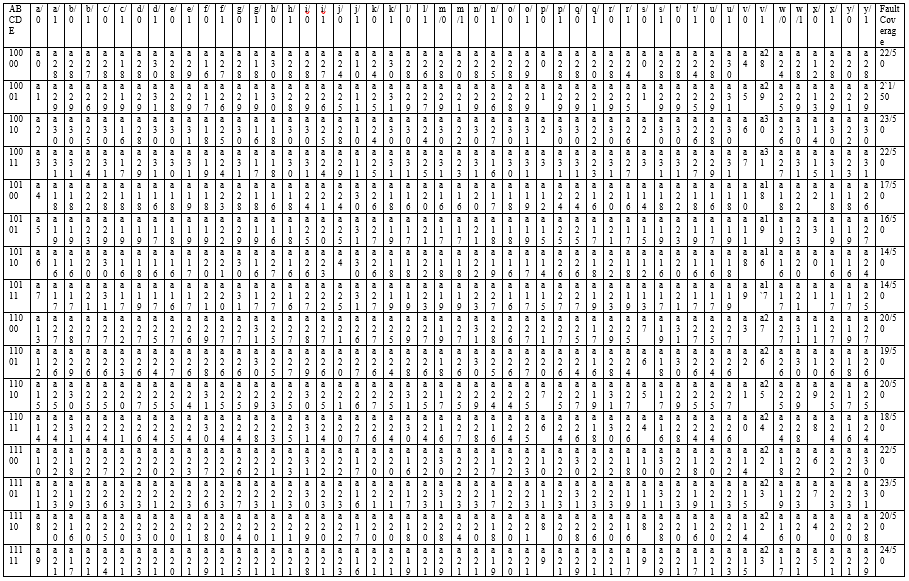
The truth table of KMD Gate4 is shown in Table 15 and its fault tolerance capability is analyzed in Table 16. Here a0 to a31 represent the position of the i/o vector.

**Table 15: Truth Table of KMD Gate4**





**Table 16: Fault tolerant table of KMD Gate4**



From the table the average Fault Tolerance of KMD Gate4 = 40.25%